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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/463,642	01/24/2000	TORU AIDA	FURUSAWA	6607

7590 03/25/2004

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EXAMINER	
HARVEY, DAVID E	
ART UNIT	**PAPER NUMBER**
2614	8

DATE MAILED: 03/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/463,642	AIDA ET AL	
	Examiner	Art Unit	
	DAVID E HARVEY	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7-9,12 and 15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-9, 12, and 15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 7-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

1) The last 9 lines of claim 7 recite:

> "wherein maximum coefficient values range from 1 or less, 1 /2 or more, 1 /2 or less, 1 /4 or more 1 /4 or less, 1/8 or more,. . ., to 0 or more".

This recitation is indefinite because it is not clear what is means and to what it refers. Clarification is required.

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida [US Patent #5,303,047] in view of Darthenay et al. [US Patent #5,923,213].

I. The showing of Yoshida:

As is shown in figure 5, Yoshida disclosed a horizontal contour emphasizing circuit that comprised:

1) An input terminal (1) for receiving a luminance signal;

2) Circuitry (3, 4) for extracting a contour emphasizing signal from the received luminance signal;

3) Luminance level detection circuitry (e.g. @ 8) for detecting the a level of the received luminance signal;

4) Variable gain circuitry (@ 7) for applying a predetermined gain (i.e. multiplying factor) to the extracted contour signal whereby the gain that is applied increases as the detected level of the received luminance signal increases (e.g. see figure 4); and

5) An adder (5) for adding the amplified contour signal to the received luminance signal to generate and output (@ 6) a contour emphasized luminance signal.

II. Differences:

Claim 12, as presently drafted, appears to differ from the showing of Yoshida only in that claim 12:

1) Processes sampled digital signaling and, thereby, utilizes digital circuitry (e.g. digital decoders and logic gates);

2) Specifies the specific structure of the variable gain circuitry. Namely, claim 12 requires the variable gain circuitry to be comprised of logic gates and multipliers for changing the emphasizing coefficients (e.g. gain factor) based on n levels of a digitized luminance signal (note applicants' figure 3).

III. Obviousness:

The following is noted:

1) Darthenay et al. has been cited because it evidences the fact that it was known to have variable gain circuitry using gates (@ 20) and multipliers (@ 10) wherein the gain factor is controlled digitally based on the level of an n-bit control signal (see figure 1).

Yoshida does not specify the configuration of his variable gain amplifier (7) and therefor one skilled in the art would have been forced to rely on the prior art for such details. The examiner maintains that Darthenay et al. fairly represents the prior art that one would have had to rely. Being such, the examiner maintains that it would have been an obvious choice of design to have implemented the VCA in Yoshida using the circuitry of conventional design that is evidenced to have been well known in the art by Darthenay et al.

2) And while the modified circuitry of Yoshida operates to process the received luminance signal in the analog domain, implementing such processing in the digital domain represents nothing more that an obvious

upgrade of technology. In the digital domain, the gating circuitry (20) of Darthenay et al. would have been implemented using a plurality of AND gates whose output feeds an OR gate (i.e. such clearly being the logical/digital domain equivalent of the illustrated switches and common node that is shown)[1].

As to the specific values of the coefficients, the examiner maintains that having selected multiples of ½ had notoriously well known advantageous and thus obvious choice of design in view that it allowed such multipliers to be implemented using shift registers. That is:

a) When a binary number is shifted one decimal place to the right it is effectively divided by two (i.e. multiplied by ½);

b) When a binary number is shifted two decimal place to the right it is effectively divided by four (i.e. multiplied by 1/4); and

[1] Gating circuitry 79 and 81 in figure 2 of DE #2,260,621 has been cited to exemplify such a well known digital implementation /configuration.

c) When a binary number is shifted three decimal places to the right it is effectively divided by eight (i.e. multiplied by 1/8).

6. Claims 15 and 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida [US Patent #5,303,047] in view of Darthenay et al. [US Patent #5,923,213] for the same reason that was set forth for claim 12 above.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAVID E HARVEY whose telephone number is (703) 305-4365. The examiner can normally be reached on M-F from 9 AM to 6PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller, can be reached on (703) 305-4795. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4700.

DAVID E HARVEY
Primary Examiner
Art Unit 2614